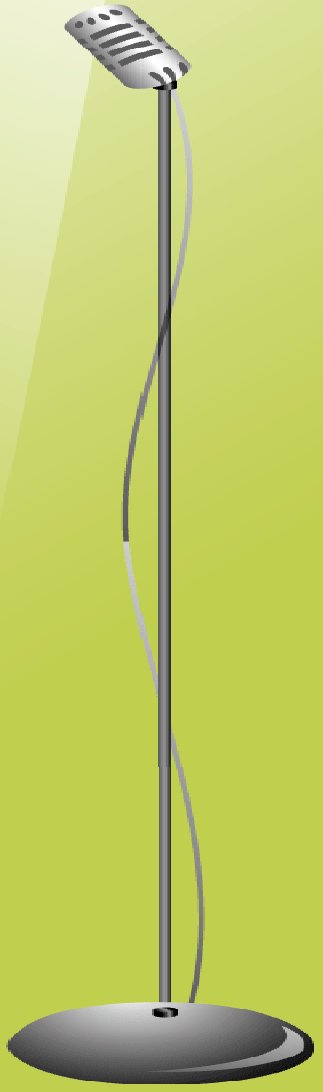
Maximizing J750 Test Cell Capacity — Lessons Learned



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Abstract

Test cost reduction will be achieved by maximizing the capacity of the test cell. Due to the variety of devices that need to be tested, a certain tester resource is always a blocking factor. This case study highlights the steps involved to increase the capability of the J750 test cell by adding external resources. In this paper, the authors will present several case studies for adding resources on the DIB, PIB, Probe Card or external. The main challenges for adding resources are highlighted in the studies. Hardware, power, software and mechanical requirements will also be addressed.

Content

1. General

1.1 Preface

This paper describes several case studies based on the lessons learned to increase the capability of a J750 test cell.

Main question of this paper is: How can the test cell capability be used to its maximum.

Our study contains both practical lessons learned during Instrument development at Salland Engineering and theoretical approaches about how maximum capability could be reached.

1.2 About the authors

Dirk Jan Stuij is project leader Instrument development and is responsible for the development of the X750 instrument. In the past Dirk Jan also has done development on HDPMU and HDACTO instruments.

Erik Kloekke is Instrument manager at Salland Engineering and is responsible for the development of new instruments for the ATE industry.

1.3 Abbreviations and terminology

Abbreviation	Description
DUT	Device under Test.
ATE	Automated Test Equipment.
HDACTO	High Density AC Test option
HDPMU	High Density PMU
PMU	Parametric Measurement Unit
BIST	Built In Self Test
DPS	Device Power Supply
PIB	Prober Interface Board
DIB	Device Interface Board
FPC	Fixed Probe Card
UPH	Units Per Hour

Table 1. Abbreviations.

Terms	Description
HDACTO	High density analog CTO. Modularie configuration up to 64 captures or sources or a mix with a multiple of 8 for FLEX™ or UltraFLEX™.
HDPMU	High density PMU up to 192 channels for FLEX or UltraFLEX.
FLEX	Teradyne tester.
J750	Teradyne tester.
IDPS750	External power supplies for J750, up to 256 channels.
X750	Add on power supplies for J750, up to 640 channels.

Table 2. Terminology.

2. Introduction

Within the ATE industry everyone wants to reach two goals:

- Get maximum units per hour (UPH).
- Reach the highest yield.

Main reason for these two goals is: **Test cost minimalization.**

Reaching the highest yield is not within the reach of the ATE engineer but mainly within wafer production process.
Maximize UPH is one of the goals all ATE engineers know.

It is an everyday challenge for ATE engineers to work on increasing test cell capacity by optimizing the test-flow, use of inventive solutions and optimal use of available equipment.

Salland Engineering uses the expertise of qualified ATE engineers divided in three main groups: Test Application, Tools and Instruments. This results in developing practical and usable solutions for the whole ATE market.

For many years, engineers built up a large experience on increasing test cell capacity with a different focus for each group:

- Test Application: development, optimization and conversion of test programs.
- Tools: Software tools and utilities for statistical analysis (SEDana) and test cell control (DTC).
- Instruments: Development and production of hardware test solutions (HDPMU, IDPS etc.).

In general, the engineers at Salland Engineering are all ‘optimization specialists.’

In this paper we share some of our experience regarding increasing test cell capacity by developing inventive hardware solutions and additional software tools.

3. Increasing test cell capacity: a short history.

During the years, several techniques are used for increasing test cell capability.
Every Application engineer is familiar with the basic techniques:

- Use parallel testing by increased site count.
- Reduce resources idle time by optimizing serial and parallel testing.
- Optimize test applications for test time reduction e.g., simplify test methods.

A second approach used to maximize the use of available tester resources like:

- Sharing tester resources for two or more sites.
- Use a reduced pin count during testing.

Another development in the past was changing the DUT to adapt Design for Test. By developing BIST functionality within the DUT, the number of resources needed for each DUT is reduced. This enables the possibility to increase the number of sites and UPH with the same available resources.

Still increased UPH is a target for new developments. When all other developments do reach to a saturation point, still one item can be addressed as a solution to increase capacity:

Increase the limited number of (critical) tester resources.

3.1 Pros and cons of adding tester resources on various ways.

There are several possibilities and challenges to add tester resources.
A short overview of the possibilities including some pros and cons:

The first way of adding resources can be done within the tester itself: Use an empty slot and add an instrument with more resources.

Pro	Con
o Very clean and integrated solution. o No external equipment needed. o Familiar maintenance and use. o No additional floor space needed.	o Open architecture required. o More resources in the same space. So High Density instrument solution is required. o Restrictions regarding defined and available number of pins. o Restrictions regarding available power and cooling within tester for each instrument. o Backwards compatibility with original Tester configuration is not possible when tester was/is full with instruments.

Table 3. Pro and con of adding resources within the tester

Some examples:

- Teradyne HDVIS (for J750).
- Teradyne APMU (for J750).
- Salland HDPMU (for FLEX).
- Salland HDACTO (for FLEX).

The second way of adding resources can be done on the DIB or PIB/FPC board by adding instrument circuitry on the load board:

Pro	Con
o Resources close to the DUT. o Less influence from environment (noise, etc.). o High speed possible between DUT and instrument. o No external equipment needed. o Flexible solution: By exchanging the Interface hardware also instruments are changed. o No additional floor space needed.	o Limited power. o Limited instrument control options within existing environment (additional communication channel could be a solution). o Specific solution on interface hardware: reusability of instrument not possible for other DUTs. o Limited space, no big numbers of resources can be added, no room for large instruments. o Limited number of added instruments.

Table 4. Pro and con of adding resources on the load board

Some examples:

- Level shifters to increase dynamic range.
- IDDq modules.
- RF modules (e.g., Power meters).
- Connection points for external instruments (e.g., PCI-e, USB).

A third way is adding a high number of externally placed instruments connected to the DIB or the PIB (External instruments in 19 inch cabinet).

Pro	Con
o External solution: no open architecture needed. o No restrictions regarding space, cooling, power etc. for instrument electronics. o Quickly backwards compatible to J750 stand alone solution. o Instrument reusability for various DUT types. o Good solution for relatively slow instruments (e.g., DPS).	o Long distance between Instrument and PIB, which can have influence on signal integrity. o Long cabling (5-6 meter) required between instrument and PIB/FPC location where DUT is tested. o Test floor occupation of cabinet. o Adding a lot of resources means adding a lot of cabling. o High quality connectors needed for connecting disconnecting during docking undocking.

Table 5. Pro and con of resource addition using a 19 inch cabinet.

Examples:
- o SE IDPS 750.
- o Standard rack and stack.

A fourth way is adding a high number of externally placed instruments connected to the DIB or the PIB (External instruments in a backpack as close as possible to the test head).

Pro	Con
o External solution: no open architecture needed. o Position closest to PIB/DIB: shortest possible high density connection between external instruments and DUT. o Backwards compatible. o Shorter distance to the DUT: possibility to develop more critical instrument types, even on high density. o Instrument reusability for various DUT types. o Less floor space: backpack is mounted within the J750 area. o Less cabling: reduction of connection issues. o Docking and undocking as on normal J750 system.	o Still some distance between Instrument and PIB, which can have influence on signal integrity for very high speed instrument solutions. o Still some test floor occupation needed of system power cabinet (solution is stacking cabinet with J750 power vault).

Table 6. Pro and con of adding tester resources by using a backpack solution.

Example:
- o Salland X750.

As seen in the proposed solutions above there are several pros and cons for each possibility.

When additional resources are needed, it is important to choose the optimal solution based on required instrument functionality, speed, density, available floor space, required flexibility and costs.

Adding resources in a high density solution does not mean that internal tester resources are multiplied. New resources are developed according to the latest available technology and can be adapted to specific needs and requirements. This enables possibilities to increase functional use of the test cell which can result in adding new instruments with new specifications and operational use.

4. Increasing test cell capacity: adding tester resources.

Over the years, engineers at Salland Engineering faced the question of increasing the number of resources on the Teradyne J750 and FLEX tester platforms.

Based on our experiences, we will share some lessons regarding four main challenges for adding tester resources:

- Development of instrument hardware add-ons.
- How to solve increased power demands.
- Solve mechanical issues.
- Development of inventive software add-ons for instrument hardware control.

Based on these topics some cases will be shown and what lessons were learned by our engineers.

4.1 Influence of adding resources on parallel efficiency

Increasing test cell capacity by adding resources has influences on parallel efficiency. Although parallel efficiency depends on more than only resources, the main target is to reduce test cost by increasing the number of sites.

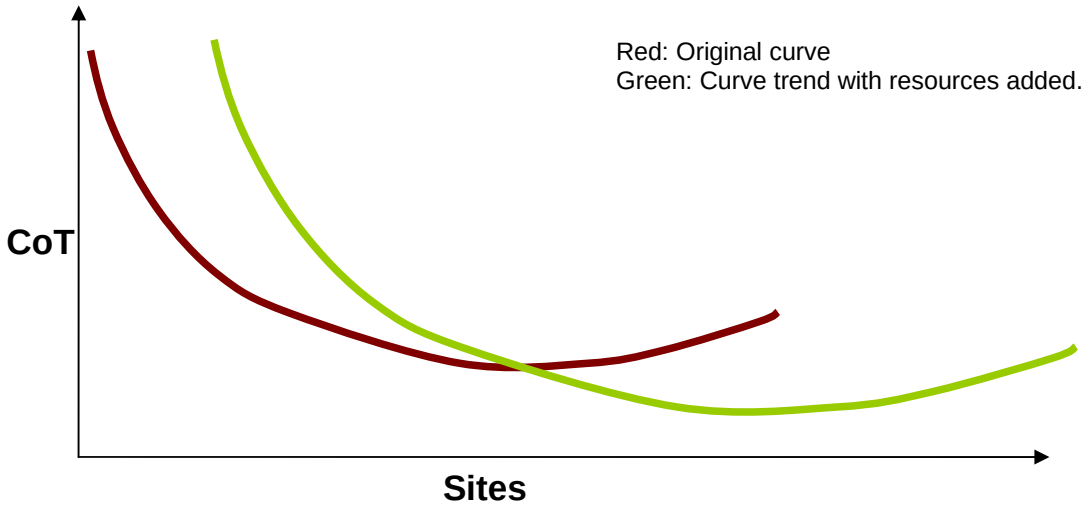

Figure 1. Influence of adding tester resources to parallel efficiency.

More information on parameters that influence parallel test efficiency is available in a 2010 TUG paper by Gregory Smith: Modeling Test Economics for High Site Count Parallel Test.

4.2 Challenges regarding instrument development.

The overall experience from Salland on electrical hardware development is collected on four instrument projects related to Teradyne tester equipment.

- IDPS750; a 265 DPS solution for J750.
- X750; a more universal solution for DPS and other instruments, also for J750.
- HDPMU; a 192 PMU solution developed for FLEX.
- HDACTO; a 64 channel AC source/capture solution, also developed for FLEX.

Developing on FLEX had advantages because:

- Instruments can be put inside the FLEX itself because the FLEX has an open architecture.
- Open Architecture enables Support from Teradyne.
- A suitable development environment was available (FLEX Test-bed).

Development on J750 is more challenging because:

- J750 does not have open architecture.
- Integration needs to be done as an add-on in relation to the existing J750 tester.
- A functional development and internal test environment also needs to be developed.
- Instrument will be a add on and the J750 system must be backward compatible.

This paper will highlight some challenges regarding development of instruments for J750.

4.3 Lessons learned during IDPS development.

After demand of our customers, Salland started some years ago with the development of the IDPS instruments.

Figure 2. J750 Test Cell with IDPS 750.

IDPS750 is a 19 inch cabinet with 128 or 256 DPS power supplies which is placed nearby a J750 tester.
The connection between the IDPS and the test head is done with cabling. Each instrument channel is individual connected to the PIB. With 256 channels it will result in a lot of cabling and connectors.
Mechanically this is a challenge and space consuming.

The size of the PIB is different in comparison with an original J750 PIB to create more space outside the J750 test head for connecting all IDPS channels.

Main challenges faced by Salland during development of IDPS:

- How to add 256 DPS channels to a J750-512 tester. It is a closed architecture.
- How can we create a compact solution nearby the J750 test head on the test floor?
- How do we connect 256 DPS channels to the DUT?
- First steps of SE developing an external instrument on J750: everything is new!

Figure 3. IDPS cable connection to the PIB.

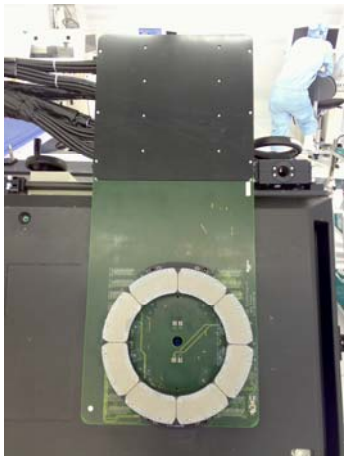

Figure 4. Bottom view IDPS-PIB with 1024 Pogo tower.

During the development path, several challenges appeared and a lot of lessons are learned by the engineers from Salland.

To overcome the issue of the closed architecture, the IDPS is developed as a separate system which is positioned next to the J750. Each instrument channel is separately connected to the PIB by using specific designed cabling and high quality connectors
To handle the increased number of connections from the PIB to the DUT, the original J750-512 pogo tower is replaced with the J750-1024 pogo tower. The additional pins are used for the IDPS channels.
On software level, the IDPS is integrated via a library (add-on) within IG-XL™. The instrument is controlled by using low level software commands.

Lessons learned in the IDPS project:

- Connecting 256 DPS channels to the test head is challenging. To provide a good connection specific instrument cable is developed and heavy duty connectors are used for connecting the cables to the test head. This solution is restricted to 256 channels because of mechanical solution.
- To make space for the connectors, a new design is made for the PIB. The docking system on J750 is modified to make room for this new designed PIB.
- More DPS channels do also mean more connections to the DUT. This is solved by using another type of Pogo Ring. In this case the J750-512 test head is working with the J750-1024 Pogo Ring. With current solution we reach about the maximum number of channel on the PIB.
- IDPS has reached the limitations of adding resources by using racks and cabling. IDPS has limitations regarding speed, accuracy and individual channel control. Main restriction is the length of the cables.

Some do's and don'ts learned with the IDPS project:

- Prevent using long cabling between instrument and DUT when high speed is required. Long cables have an influence on signal integrity.
- Use good guiding for the cabling to prevent cable damage or connection issues.
- When the solution needs to be certified for CE (safety and EMC) it is better to divide the instrument into a power section which is certified for safety and an instrument section which is certified for EMC. This is easier for the certification process.
- Effective use of the instrument will be easier when more attention is put into the software integration. J750 application engineers do use a lot of templates and are not always familiar with using a programming language for instrument control.

With 50+ systems into the field, we can conclude that IDPS is a success.

4.4 Lessons learned during X750 DPS development.

Because of increasing demand for more resources on J750, Salland has developed a more flexible solution which can be used for J750: the X750.

Within the X750 project, Salland solved the main limitations of the IDPS instrument: increase speed, accuracy, more power and enable individual channel control.

Challenges for X750 were:

- Increase DPS power, speed and accuracy.
- Increase number of DPS channels (256++).
- Reduce mechanical issues (connecting and disconnecting cabling).
- Keep used floor space, or use less.
- Create flexibility regarding instrument add-ons.
- Improve integration into existing development environment (Application level).

Based on these challenges, Salland started developing the X750 for J750.

Figure 5. J750 combined with X750 system.

X750 is a small ‘backpack’ style solution which is mounted directly on the J750 test head. The X750 can house up to 10 different instrument boards which can be connected to the DUT by using signal boards. The instrument control interface is based on PCI-e. The instruments are powered by using a small system power supply which is placed nearby.

X750 and J750 are completely independent. Both instruments are merged together on Load board level. Controlling is done by using the PCI-e interface. This communication path is done by using an optical cable to optimize signal quality and prevent ground loops over this path.

See Figure 6 for a schematic overview of the J750/X750 combination.

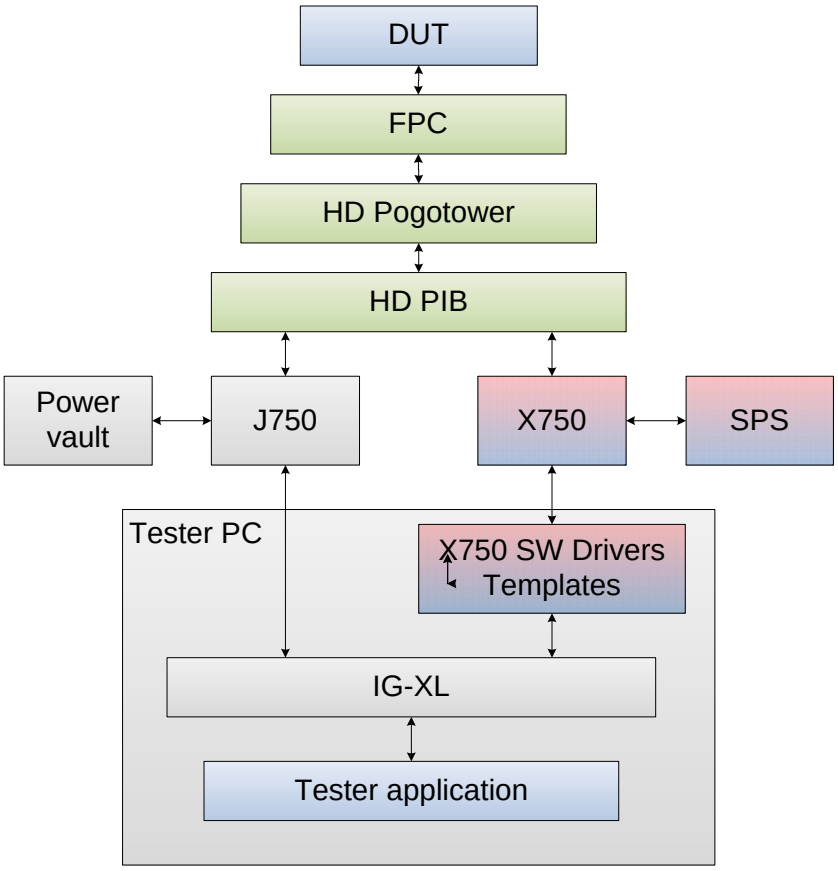

Figure 6. Schematic overview of J750 with X750.

During X750 development, Salland Engineering solved the following issues and the lessons learned are:

- Create an innovative new solution: an instrument backpack as close as possible with the J750 and the test head without influencing the J750 see paragraph 4.6.
- Add modularity and flexibility: Solved by defining universal instrument slots.
- Increase speed and flexibility regarding instrument control: use of PCI-e and efficient and flexible grouping mechanisms.
- Compress instrument footprint: 512-640 DPS instruments (400-800mA each) into the X750 backpack. This will require extreme cooling capacity. See paragraph 4.5.
- Easy docking and undocking: No heavy connectors and big bunches of cable, only one power cable and a optical communication cable.
- Completely backwards compatible by removing 4 parts of the X750 system and the J750 can be used into its original state.
- More connections to the test head by using a high density pogo tower (from 2992 pins up to 5848 pins). The challenge here was the pressure needed for the whole tower to make good contact. Solved by low-force pogo pins.
- Suitable for use with the J750-512 and J750-1024 test head.

Some do's and don'ts based on our X750 experience:

- Adding a backpack to a J750 tester also interferes with the mechanical environment of the J750 test head. The gap between the J750 air outlet and the backpack needs to be chosen carefully. Advice is to use the air diverter between the J750 and X750 backpack.
- A backpack adds weight to the test head. The manipulator or hinge needs to be suitable for this added weight.
- Test cell migration by adding X750 is like a customer specific solution. So it is important to know the current test cell configuration. By doing an accurate customer survey this migration is be easier to do.
- Pogo pins are very useful for creating a high density connection between the X750 signal boards and the PIB/DIB. It is important that the thickness of the signal boards is within a certain accuracy. To reach this, special attention is needed during production of this PCB.

4.5 Solve increased power demand.

During the years, Salland learned that one of the major things in adding tester resources is the increased power demand.

It is reasonable: if you want to test more of the same in parallel, you need more resources for power: the total power demand increases.

In addition, another issue is ongoing: Voltages needed for power are going down, and required current rises. For higher current more power is needed from the DPS instruments.

Based on these two facts, Salland has developed solutions to fit the increased power demand.

Challenges are:

- Using low voltages and higher current requires more dissipation capability for DPS instruments. Mainly because of the linear architecture of the instrument.
- With increased supply current more attention is needed for the path between DPS and DUT to compensate loss.

During the X750-DPS development, Salland has learned several lessons regarding the needed power:

- Choosing a non-linear DPS solution is not a preferred option due to higher noise which requires more filtering.
- The loss over the power circuitry to the DUT is significant when high current is required. This needs to be controlled and compensated by using efficient sensing and enough overhead of the DPS ranges.
- When high current is required, a linear DPS dissipates more. This increases instrument dissipation, which can interfere with instrument behavior. By increasing cooling capacity and the use of multiple power levels for feeding the end stage of the DPS instrument, this effect can be minimized.
- The X750 solution requires a lot of power. It is not possible to use standard power conversion equipment. A separate System Power Conversion cabinet is developed.
- A separate power conversion cabinet needs to comply with local safety rules and regulations. Additional safety circuitry is added.

Some do’s and don’ts regarding power conversion:

- When a more universal power conversion is engineered, be aware that multiple input voltages are used around the world.
- On X750 a high current connection is used between the backpack and the power conversion cabinet. To prevent that this high current damages other equipment within the test cell, this current is guarded with additional sense connections.
- It is difficult to find out what the root cause is when the J750 or the backpack is switched off into an error situation. To find the root cause faster, both the IDPS and the X750 power cabinet are using monitoring circuits. Status is saved in memory and available for analysis.
- IDPS and X750 are using field replaceable power supply units for down time reduction.

4.6 Solve mechanical issues.

Adding resources has influence on the mechanical environment of the test cell.

The IDPS was a large test cell modification, mainly because of the bunch of cables and the challenge of connecting 256 IDPS instruments to the test head.

In short, Salland faced the following challenge:

- How to connect the IDPS mechanical to the DUT?

Some solutions Salland has implemented into IDPS:

- A modified PIB is used to enable the possibility to add connectors for connecting IDPS to the test environment.
- Because this specific PIB is heavy and large, this solution is limited to 256 channels. (Figure 3 gives an indication about how heavy this is.)
- To handle the increased number of resources, the J750 (in this case the 512 test head) uses the 1025 pogo tower. The additional pins are used for the IDPS channels.
- IDPS cabling needs to be disconnected when the system is undocked from the prober.

During X750 development, we want to mechanically improve and solve issues which appeared during development of IDPS.

Challenges from Salland during X750 development:

- Do not use cabling anymore between instrument and DUT. It reduces possible connection issues.
- Enable possibility to use X750 on a J750-1024 test head.
- Reduce required floor space.

Based on these challenges, Salland engineered the following solutions:

- By positioning the X750 as near as possible to the test head, all signal cabling can be replaced with signal boards: a compact PCB solution. Only a power cable and communication cable are needed. No need to disconnect.
- Replacing the connectors to the PIB by pogo blocks, increases the connection density and enables connection of 512 or more DPS instruments to the PIB. It also adds flexibility of the test cell. If the additional resources are not needed, these pogo blocks are removed and the test cell behavior is as before the resources are added (100% backward compatible).
- Using a specific developed high density Pogo tower, it is possible to connect 512+ DPS channels including the full 1024 J750 test head to the FPC. Density of the tower has increased to 5096 pins. When current pogo pins where used the pressure needed for good contact became too high for some probers. There for low force pogo-pins where used.
- For this new pogo tower a new debug tool is developed for debugging with the FPC. This tool was required for easy use and forcing a good contact pressure by hand.

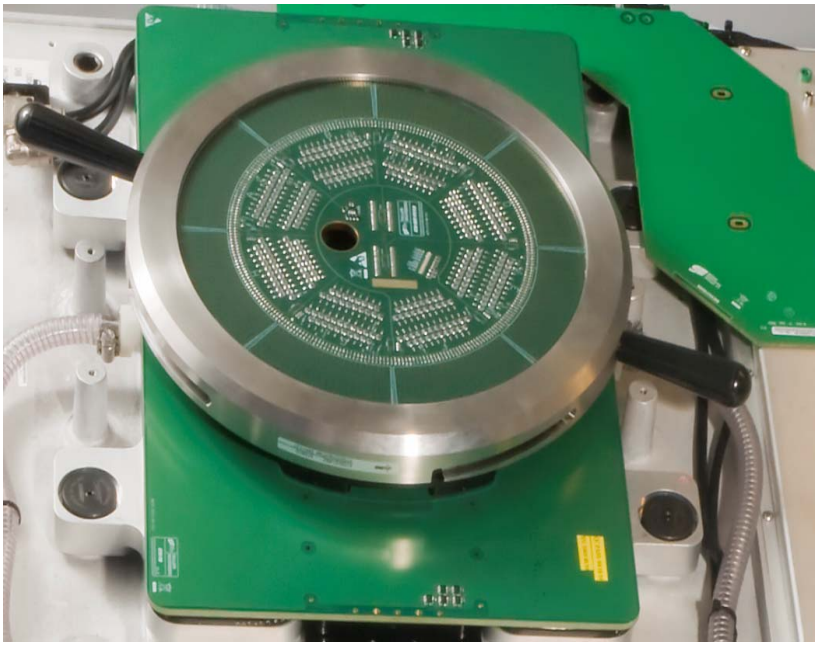

Figure 7. High density PIB, Pogo Tower, FPC and Debug tool for X750.

Do's and don'ts regarding mechanical issues on adding resources:

- Increasing the number of pogo pins, also increases the needed force for connecting boards to these pins. This force can be reduced by using low force pogo pins with a specific designed connection point.
- Because the pogo pins also change the way force is spread over the load boards, it is needed to add a board stiffener when the load board is not thick enough.
- Replacing a standard pogo tower with a high density one is expensive and not always needed. On several types of pogo towers, it is possible to exchange only the required segments with high density segments.

4.7 Improve software integration for added instruments.

A good integration of new resources not only consists of developing hardware and solving power and mechanical issues, it also needs suitable software integration.

Software development for IDPS and X750 also means a good integration within the existing software environment. For J750 this is IG-XL.

During IDPS development the integration is done on a low level. A basic low level software driver is developed, and the commands used for controlling the IDPS system are integrated by hand within the application software.

One of the lessons learned regarding this, is that the use of new resources is easier when the required software is integrated on a higher level.

During X750 instrument development the software integration has reached the next level (seamless integration).

For X750 level sheet, pin-map sheet and test template integration is developed. This makes development with X750 more equal to the normal development on J750.

More information about improvements on software integration can be found into a 2010 TUG paper by Gerko de Roo titled: High Channel Count External Instrument Integration with J750.

In addition, more attention is put into enabling high parallel use of the whole X750 system. All channels can be controlled in parallel within hardware. Site handling is added in the instrument, and individual control of sites/DPS channels is possible.

X750 DPS debug panels are available for engineering.

The High Parallel Test solution (HPT) enables the possibility to handle more than 32 sites on J750. Because HPT normally handles channels sequentially, adding a lot of resources like DPS affects parallel efficiency negatively.
To reduce the influence of added resources, the X750 driver is site-aware. This means that it is not necessary to sequentially loop through the X750 channel lists. Site-awareness of the driver reduces the need for sequential channel handling and therefore positively affects parallel efficiency.
All other J750 tester resources still require software site handling like HPT to be able to test above 32 sites.

On maintenance level parallelism is also optimized. The X750 uses a separate maintenance environment which can be used in parallel with the original J750 maintenance environment. This enables the possibility to run maintenance on both the J750 and the X750 in parallel.

Lessons learned on improved software integration:

- Software integration is more than only writing a driver which can be used for programming. IDPS was a ‘driver only solution’. Using IDPS means knowing how to programmatically use IG-XL. Within the X750 project, this usability part has improved.
- Keep software on the same level as the existing software. It is easier for the Application engineer to integrate the additional resources within the application software environment.
- Do not lose focus on the main target, even when HPT is used. Adding a lot of resources results in increase of test time because of sequential behavior of HPT. Parallel control of added resources prevent this from occurring.

5. Conclusion.

During the years, test cell capacity continuously increased when optimizing for speed, by means of integrating tests within the DUT, other test optimization solutions and tools.

Reaching the limits of available resources within the test cell itself can be resolved by adding external tester resources to increase test cell capacity.

Lessons learned by Salland tell us that adding resources is an effective possibility to increase capacity, but has some challenges on electrical, power, mechanical and software integration.

With the right environment, the right resources and the right focus it is very effective in increasing throughput and test cost reduction.

Due to future trends it is expected that adding more test intelligence on the DUT, will simplify the tester environment. By increasing the number of critical resources like DPS channels, the possibility is created for further site-increase and further maximizing test cell capacity.